UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,675	07/14/2000	Jagannath P. Agrawal	42390.P9070	6967

7590 08/18/2004

Seth Z. Kalson
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
7th Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2665	5

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,675	AGRAWAL, JAGANNATH P.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it exceeds 150 words. In addition, "A asynchronous" in line 1 should be changed to "An asynchronous". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 6, 9-12, 14, 15, 17-21, 23, 24, and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Agrawal (USPN 5,636,210).

4. Regarding claim 1, Agrawal discloses an asynchronous transfer mode switch comprising: a set of m (m=64) input ports to receive cells (Fig. 5 and col. 3, line 39-col. 4, line 34); a set of n buffer groups (n=80: 64 regular buffer groups and 16 overflow buffer groups) (ref: 23 and 27: regular and overflow buffer groups, respectively), each buffer group comprising a set of buffers, where n > m (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46); an input-to-buffer switching module to switch a cell received at one of the m input ports to one of the n buffer groups (ref. 29) (col. 9, line 52-col. 10, line 10); a set of output ports (Fig. 5 and col. 3, line 39-col. 4, line 34); and an output switching module to switch cells stored in the sets of buffers within the buffer groups to the set of output ports (ref. 32) (col. 11, lines 16-28).

5. Regarding claim 4, referring to claim 1, Agrawal discloses that the output switching module is a single stage crossbar switch (col. 11, lines 16-28).

6. Regarding claim 6, referring to claim 1, Agrawal discloses that each buffer within the sets of buffers is a 1-cell buffer (Fig. 5 and col. 8, lines 30-40).

7. Regarding claim 9, referring to claim 1, Agrawal discloses a first memory device to store n data structures (single buffer address in the pool), wherein there is a one-to-one correspondence between the data structures and the buffer groups, wherein each data structure indicates buffers within its corresponding buffer group available for storing new cells (col. 11, lines 29-65).

8. Regarding claim 10, referring to claim 9, Agrawal discloses that the n data structures are bit-maps (col. 11, lines 29-65 and col. 12, lines 23-33).

9. Regarding claim 11, referring to claim 9, Agrawal discloses a second memory device to store nk CNT field values, wherein there is a one-to-one correspondence between the CNT field values and the buffers, wherein a CNT field value indicates a number of output ports to read its corresponding buffer (col. 12, lines 27-33 and col. 12, lines 53-67).

10. Regarding claim 12, referring to claim 1, Agrawal discloses a first memory device (buffer management module for regular buffers) to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell (col. 11, line 29-col. 12, line 33, esp. col. 11, lines 39-55 and col. 11, line 66-col. 12, line 10) where the address of the group includes the bit sequence b0b1...b7 which indicate which buffers in the group are available.

11. Regarding claim 14, referring to claim 12, Agrawal discloses a second memory device (buffer management module for overflow buffers) to store n bit maps, wherein there is a

one-to-one correspondence between the bit maps and the buffer groups, wherein each bit map indicates buffers within its corresponding buffer group available for storing new cells (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65 and col. 12, lines 23-42).

12. Regarding claim 15, referring to claim 14, Agrawal discloses a third memory device to store nk CNT field values, wherein there is a one-to-one correspondence between the CNT field values and the buffers, wherein a CNT field value indicates a number of output ports to read its corresponding buffer (col. 12, lines 27-33 and col. 12, lines 53-67).

13. Regarding claim 17, Agrawal discloses a switching engine comprising: a set of input ports to receive cells (Fig. 5 and col. 3, line 39-col. 4, line 34); a set of buffer groups (ref: 23 and 27: regular and overflow buffer groups, respectively), each buffer group comprising a set of buffers, the set of buffer groups greater in number than the set of input ports (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46) where the number of input ports is 64 and the number of buffer groups is 80 (64 regular buffer groups and 16 overflow buffer groups); an input-to-buffer switching module (ref. 29) to switch cells received at the input ports to the sets of buffers within the set of buffer groups, wherein each switched cell is stored in one buffer within one buffer group (col. 9, line 52-col. 10, line 10); a set of output ports (Fig. 5 and col. 3, line 39-col. 4, line 34); and an output switching module (ref. 32) to switch cells stored in the sets of buffers within the buffer groups to the set of output ports (col. 11, lines 16-28).

14. Regarding claim 18, referring to claim 17, Agrawal discloses a memory device to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell, wherein all stored buffer group addresses in the memory device are indicative of buffer groups having at least one buffer available to store a new data cell (col. 11, line 29-col. 12, line

33, esp. col. 11, lines 39-55 and col. 11, line 66-col. 12, line 10) where the address of the group includes the bit sequence b0b1...b7 which indicate which buffers in the group are available in the pool of available buffers.

15. Regarding claim 19, referring to claim 17, Agrawal discloses a memory device to store bit maps indicative of buffer states within the set of buffer groups (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65 and col. 12, lines 23-42).

16. Regarding claim 20, referring to claim 17, Agrawal discloses a memory device to store CNT field values corresponding to cells stored in the buffers within the set of buffer groups, wherein a CNT field value associated with a stored cell is indicative of a number of output ports to read the stored cell (col. 12, lines 27-33 and col. 12, lines 53-67).

17. Regarding claim 21, referring to claim 17, Agrawal discloses a first memory device to store buffer group addresses indicative of which buffer groups have a buffer available to store a new data cell, wherein all stored buffer group addresses in the first memory device are indicative of buffer groups having at least one buffer available to store a new data cell (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65; col. 11, line 66-col. 12, line 10; and col. 12, lines 23-42); a second memory device to store bit maps indicative of buffer states within the set of buffer groups (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65 and col. 12, lines 23-42); and a third memory device to store CNT field values corresponding to cells stored in the buffers within the set of buffer groups, wherein a CNT field value associated with a stored cell is indicative of a number of output ports to read the stored cell (col. 12, lines 27-33 and col. 12, lines 53-67).

18. Regarding claim 23, Agrawal discloses a switching engine to switch cells from input ports to output ports, the switching engine comprising: an input processing module to attach

routing tags to cells (col. 8, line 57-col. 9, line 40); a set of buffer groups, wherein each buffer group comprises a set of buffers to store cells (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46); and a buffer management module comprising a first memory device to store pointers to (addresses of) those buffer groups having at least one available buffer to store a new cell (col. 11, line 66-col. 12, line 10); wherein the input processing module is coupled to the buffer management module to send buffer allocation requests to the buffer management module, wherein in response to a buffer allocation request the buffer management module shifts out a pointer stored in the first memory device (col. 11, line 29-col. 12, line 46, esp. col. 11, line 66-col. 12, line 22 and col. 12, lines 34-42).

19. Regarding claim 24, referring to claim 23, Agrawal discloses that the number of buffer groups within the set of buffer groups is greater than the number of input ports (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46) where the number of input ports is 64 and the number of buffer groups is 80 (64 regular buffer groups and 16 overflow buffer groups).

20. Regarding claim 26, referring to claim 23, Agrawal discloses that each buffer group has a state indicative of which of its buffers are available to store a new cell, the buffer management module further comprising: a second memory device to store bit maps indicative of the states of the set of buffer groups (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65 and col. 12, lines 23-42).

21. Regarding claim 27, referring to claim 26, Agrawal discloses that the buffer management module further comprises: a buffer allocation module to allocate buffers in response to buffer allocation requests, wherein the buffer allocation module receives a bit map stored in the second memory device at a location indicated by the shifted-out pointer, provides a buffer number

pointing to a bit position within the bit map indicative of an available buffer in the buffer group pointed to by the shifted-out pointer to store a new data cell, and updates the bit map by changing the bit position value to indicate a new state of the buffer group pointed to by the shifted-out pointer (col. 11, line 29-col. 12, line 46, esp. col. 11, lines 39-65 and col. 12, lines 23-42).

22. Regarding claim 28, referring to claim 27, Agrawal discloses that in response to the buffer allocation request, the buffer management module sends to the input processing module the shifted-out pointer and the buffer number, and the input processing module attaches a routing tag to a cell indicative of the shifted-out pointer and the buffer number (col. 8, line 57-col. 10, line 10, esp. col. 9, lines 59-64 and col. 10, lines 5-8 and col. 11, line 29-col. 12, line 46, esp. col. 12, lines 4-10).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 2, 3, 5, 7, 8, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal (USPN 5,636,210) as applied to claim 1 above, and further in view of Kamaraj et al. (USPN 6,501,757).

25. Regarding claim 2, referring to claim 1, Agrawal does not expressly disclose that the input-to-buffer switching module is a single stage m by n crossbar switch; however, Agrawal does disclose that the input-to-buffer switching module is a banyan router (Fig. 5). Kamaraj

teaches, in an ATM switch, using a crossbar switch in place of a banyan router since the crossbar switch is smaller and dissipates less power (col. 4, lines 48-54 and col. 6, lines 37-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input-to-buffer switching module be a single stage m by n crossbar switch since a crossbar switch is smaller and dissipates less power than a banyan router.

26. Regarding claim 3, referring to claim 1, Agrawal does not expressly disclose that the input-to-buffer switching module is a multi-plane crossbar switch; however, Agrawal does disclose that the input-to-buffer switching module is a banyan router (Fig. 5). Kamaraj teaches, in an ATM switch, using a crossbar switch in place of a banyan router since the crossbar switch is smaller and dissipates less power (col. 4, lines 48-54 and col. 6, lines 37-46). Kamaraj also teaches using multiple planes in a switch in order to transform a smaller switch into a larger switch (col. 7, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input-to-buffer switching module be multi-plane crossbar switch since a multi-plane crossbar switch is smaller and dissipates less power than a banyan router and exhibits modularity such that the switch can be expanded.

27. Regarding claim 5, referring to claim 1, Agrawal does not expressly disclose that the output-switching module is a multi-plane crossbar switch; however, Agrawal does disclose that the output-switching module is a crossbar switch (Fig. 5). Kamaraj teaches, in an ATM switch, using multiple planes in a switch in order to transform a smaller switch into a larger switch (col. 7, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the output-switching module be a multi-plane crossbar switch since a multi-plane crossbar switch exhibits modularity such that the switch can be expanded.

28. Regarding claims 7 and 16, referring to claims 1 and 15, Agrawal discloses that each buffer group comprises a set of k buffers (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46) where k is equal to eight for the regular buffers and k is equal to 4 for the overflow buffers, the input-to-buffer switching module further comprising: a set of n 1 by k demultiplexers (Fig. 5 and col. 9, line 52-col. 10, line 10) where k is equal to eight for the regular buffers and k is equal to 4 for the overflow buffers; and at least one switch to switch a cell received at one of the m input ports to one of the set of n 1 by k demultiplexers (Fig. 5 and col. 9, line 52-col. 10, line 10); wherein each 1 by k demultiplexer is coupled to one of the set of n buffer groups to store each cell switched by the at least one crossbar switch into one buffer (Fig. 5 and col. 9, line 52-col. 10, line 10). Agrawal does not expressly disclose that the switch is a crossbar switch; however, Agrawal does disclose that the input-to-buffer switching module is a banyan router (Fig. 5). Kamaraj teaches, in an ATM switch, using a crossbar switch in place of a banyan router since the crossbar switch is smaller and dissipates less power (col. 4, lines 48-54 and col. 6, lines 37-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the input-to-buffer switching module be a single stage m by n crossbar switch since a crossbar switch is smaller and dissipates less power than a banyan router.

29. Regarding claim 8, referring to claim 7, Agrawal in view of Kamaraj discloses that each buffer within the sets of buffers is a 1-cell buffer (Agrawal: Fig. 5 and col. 8, lines 30-40).

30. Claims 13, 22, 25, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal (USPN 5,636,210).

31. Regarding claims 13 and 22, referring to claims 12 and 21, Agrawal does not expressly disclose that the first memory device is a FIFO such that all stored buffer group addresses in the

first memory device are indicative of buffer groups having at least one buffer available to store a new data cell; however, Agrawal does disclose that the first memory device stores buffer group addresses which are indicative of buffer groups having at least one buffer available to store a new data cell (col. 11, line 29-col. 12, line 33, esp. col. 11, lines 39-55). Agrawal also discloses that FIFOs are well-known memory devices (col. 9, lines 49-51). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the first memory device be a FIFO, such that all stored buffer group addresses in the first memory device are indicative of buffer groups having at least one buffer available to store a new data cell, since FIFOs are well known memory devices.

32. Regarding claim 25, referring to claim 23, Agrawal does not expressly disclose that pointers shifted out of the first memory device are returned to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell; however, Agrawal does disclose that the pointer (addresses) shifted out of the memory device are returned to the memory device (col. 11, line 29-col. 12, line 46, esp. col. 11, line 66-col. 12, line 22 and col. 12, lines 34-42). Agrawal also discloses that the buffer allocation mechanism allocates a buffer address from the pool of empty buffers (col. 11, line 66-col. 12, line 22). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to return the pointers shifted out of the first memory device to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell in order to maintain a pool of empty buffers.

33. Regarding claim 31, Agrawal discloses an asynchronous transfer mode switch comprising a switching engine to switch cells from input ports to output ports, the switching

engine comprising: an input processing module to attach routing tags to cells (col. 8, line 57-col. 9, line 40); a set of buffer groups, wherein each buffer group comprises a set of buffers to store cells (Fig. 5; col. 8, lines 15-60; and col. 12, lines 34-46); and a buffer management module comprising a first memory device to store pointers to (addresses of) those buffer groups having at least one available buffer to store a new cell (col. 11, line 66-col. 12, line 10); wherein the input processing module is coupled to the buffer management module to send buffer allocation requests to the buffer management module, wherein in response to a buffer allocation request the buffer management module shifts out a pointer stored in the first memory device (col. 11, line 29-col. 12, line 46, esp. col. 11, line 66-col. 12, line 22 and col. 12, lines 34-42). Agrawal does not expressly disclose that pointers shifted out of the first memory device are returned to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell; however, Agrawal does disclose that the pointer (addresses) shifted out of the memory device are returned to the memory device (col. 11, line 29-col. 12, line 46, esp. col. 11, line 66-col. 12, line 22 and col. 12, lines 34-42). Agrawal also discloses that the buffer allocation mechanism allocates a buffer address from the pool of empty buffers (col. 11, line 66-col. 12, line 22). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to return the pointers shifted out of the first memory device to the first memory device if and only if buffer groups pointed to by the shifted-out pointers have at least one available buffer to store a new cell in order to maintain a pool of empty buffers.

34. Regarding claim 32, referring to claim 31, Agrawal discloses that the number of buffer groups within the set of buffer groups is greater than the number of input ports (Fig. 5; col. 8,

lines 15-60; and col. 12, lines 34-46) where the number of input ports is 64 and the number of buffer groups is 80 (64 regular buffer groups and 16 overflow buffer groups).

35. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal (USPN 5,636,210) as applied to claim 27 above, and further in view of Ash et al. (USPN 5,130,982).

36. Regarding claim 29, referring to claim 27, Agrawal suggests that the buffer management module further comprises: a module that determines if there is at least one available buffer in the buffer group pointed to by the shifted-out pointer or if there is no available buffers in the buffer group pointed to by the shifted-out pointer (col. 11, line 66-col. 12, line 22) since Agrawal discloses that the pointer (addresses) shifted out of the memory device are returned to the memory device (col. 11, line 29-col. 12, line 46, esp. col. 11, line 66-col. 12, line 22 and col. 12, lines 34-42) and that the buffer allocation mechanism allocates a buffer address from the pool of empty buffers (col. 11, line 66-col. 12, line 22). Agrawal does not expressly disclose a return flag module to set a return flag associated with the shifted-out pointer to a first value if the new state indicates at least one available buffer in the buffer group pointed to by the shifted-out pointer, and to a second value different from the first value if the new state indicates no available buffers in the buffer group pointed to by the shifted-out pointer. Ash teaches, in a communication network, using a flag to indicate if a resource is being returned to a pool of resources (col. 7, lines 35-36) where it is implicit that this is done in order to signal to the system a change in a resource. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a return flag module to set a return flag associated with the shifted-out pointer to a first value if the new state indicates at least one available buffer in the buffer group pointed

to by the shifted-out pointer, and to a second value different from the first value if the new state indicates no available buffers in the buffer group pointed to by the shifted-out pointer in order to indicate to the system whether a pointer should be returned to the pool or not.

37. Regarding claim 30, referring to claim 29, Agrawal in view of Ash discloses that the first memory device is coupled to the return flag module to store the shifted-out pointer if and only if its associated return flag is the first value (Agrawal: col. 11, line 29-col. 12, line 46 and Ash: col. 7, lines 35-36).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (703)305-6970. The examiner can normally be reached on Mon.-Fri. 7:00-5:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703)308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel J. Ryman
Examiner
Art Unit 2665

Daniel J. Ryman DJR

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600